Relaxed silicon–germanium-on-insulator substrates by oxygen implantation into pseudomorphic silicon germanium/silicon heterostructure

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(Received 16 December 2002; accepted 18 February 2003)

We have developed a modified separation-by-implantation-of-oxygen (SIMOX) process for fabricating relaxed silicon–germanium-on-insulator (SGOI) substrates without using thick graded SiGe buffer structures. Oxygen ions are implanted into a pseudomorphically grown 115 nm $Si_{0.86}Ge_{0.14}$ layer, with the implant peak located slightly below the heterostructure interface. Following two annealing processes ($\sim 800+1350\,^{\circ}C$) instead of conventional one-step annealing ($\sim 1350\,^{\circ}C$) in traditional SIMOX, a buried silicon dioxide layer is created near the original SiGe/Si interface, resulting in a fully relaxed SGOI structure. Our results show that an annealing step at a moderate temperature ($\sim 800\,^{\circ}C$) leads to less Ge loss. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1567807]

Strained Si with in-plane tensile strain is a promising material for the *p* and *n* channels of high performance metal–oxide–semiconductor field-effect transistors (MOSFETs) due to enhanced hole and electron mobilities.[1] Relaxed SiGe has been chosen as the most appropriate stressor to realize strained Si structures because of its larger lattice parameter than Si and excellent compatibility with the present silicon integrated circuit technology. In order to overcome the lattice misfit between relaxed SiGe and bulk Si, a thick compositionally graded SiGe buffer is widely used to improve the quality of the top relaxed SiGe layer.[2] Unfortunately, a thick buffer layer causes many problems such as difficulties in scaling down the sizes of devices and degradation of device performance on account of the high density of dislocations in the buffer layer. Recently, relaxed SiGe-on-insulator (SGOI) has attracted great interest due to the possibility to obtain strained Si structures.[3–7] Using SGOI substrates, strained-Si-channel *n*- and *p* MOSFETs with enhanced electron (60%) and hole (30%) mobilities have been demonstrated.[3] Furthermore, the technique combines the advantages of silicon-on-insulator (SOI) and SiGe technologies.

Separation-by-implantation-of-oxygen (SIMOX),[4,5] ion-cut (or commercially Smart-Cut)[1,6] and bonding-and-etching-back (BESOI),[7] the three main methods to fabricate SOI materials, have been explored for SGOI structures. Almost all previous studies have commenced with a thick graded buffer layer on the order of $\sim \mu$m to fabricate the SGOI structures. However, the total thickness of the SGOI film and the strained Si layer grown on SGOI must be less than 30 nm in order to scale the MOSFETs down to gate lengths of $L_g < 100$ nm in fully depleted mode.[8,9] Furthermore, in SIMOX, the buffer layer causes two severe problems besides the high cost. First, with the buffer layer, the implanted oxygen is located in the SiGe layer (top SiGe or buffer), and Ge is rejected from the oxygen-rich region and so a silicon dioxide buried layer rather than germanium oxide is formed. For high Ge concentrations, this process is not feasible and so there is an upper limit of about 14% Ge in SiGe SIMOX.[10] Second, the thick buffer layer complicates the choice of the annealing temperature. The reduced melting point of SiGe with higher Ge concentration allows lower annealing temperature, whereas the formation of buried silicon dioxide layer requires higher temperature ($\sim 1350\,^{\circ}C$) because of Ge rejection during annealing.[10]

In this letter, we report a promising technique to fabricate SGOI substrates starting with thin pseudomorphic SiGe material with no buffer layers. We adopt a modified SIMOX process by introducing two-step thermal annealing to suppress Ge loss, which results in a fine SGOI structure. Figure 1 illustrates the process to fabricate the SGOI structures. A 115 nm (note that this thickness is the smallest one reported for SGOI fabrication up to now) SiGe film with a uniform Ge composition of 14% was pseudomorphically grown on Si (100) without a buffer layer [Fig. 1(a)]. In our experiments, an additional 8 nm Si cap layer (not shown in Fig. 1) that would be oxidized in subsequent annealing was also grown

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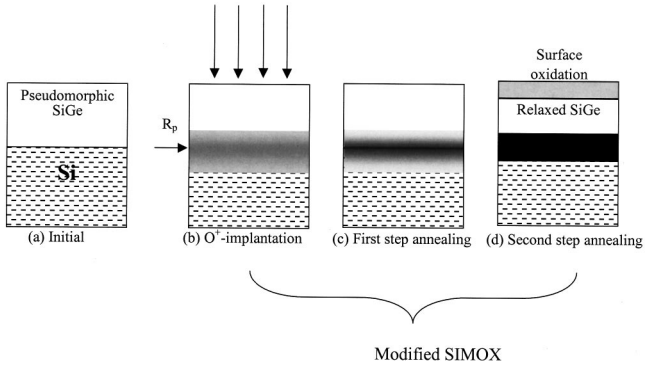

FIG. 1. Fabrication steps of SGOI structures starting from thin pseudomorphic SiGe: (a) 115 nm strained $Si_{0.86}Ge_{0.14}$ without buffer layer is grown directly on a (100) Si substrate, using an UHVCVD reactor; (b) 3×10^{17} cm^{-2} at 60 keV oxygen ions are implanted with the projected range slightly below the SiGe/Si interface; (c) annealing at a moderate temperature of 800 °C for 6 h or 900 °C for 5 h under Ar with 1% O_2; (d) high temperature (1350 °C) annealing is carried out under Ar with 3% O_2.

to prevent SiGe from possible sputtering during ion implantation. The film was fabricated in an ultrahigh vacuum chemical vapor deposition (UHVCVD) system at 500 °C with Si_2H_6 and GeH_4 precursors. The samples were then implanted with oxygen at a substrate temperature of 550 °C at a tilt angle of 7° to reduce channeling [Fig. 1(b)]. The ion energy was 60 keV and the dose was 3×10^{17} cm^{-2}. The projected range of oxygen determined using TRIM is slightly below the SiGe/Si heterostructure interface, which is different from previous reports. Afterwards, as shown in Fig. 1(c), samples were annealed in argon with 1% O_2 at 800 °C for 6 h or 900 °C for 5 h. The last step was conventional high temperature annealing at 1350 °C for 5 h under Ar with 3% O_2. After these two annealing steps, the absorption band at $\sim$1000 cm^{-1} in Fourier-transform infrared spectroscopy results (not shown in this letter) shows a transformation from a broad band for the as implanted sample (it can be deconvoluted into two subpeaks at 990 and 1080 cm^{-1}, respectively) to a single narrow peak at 1080 cm^{-1} for the annealed sample. This confirms the transition of oxygen-implantation-induced oxide from silicon suboxide to silicon dioxide.[11] No Ge oxide can be detected suggesting fine buried silicon dioxide layer formation.

Figure 2 depicts the elemental depth profile acquired by Auger electron spectroscopy (AES) of the sample annealed at 800 °C+1350 °C. A good SiO_2/SiGe/SiO_2/Si structure is revealed. The surface oxide that is about 48 nm originates from oxidation during high temperature annealing (1350 °C), indicating that the top Si cap layer has been completely oxidized and a small thickness of SiGe has been consumed. The remaining SiGe layer is about 70 nm thick with a Ge content of about 8%. It is smaller than the original Ge content due to Ge penetration through the buried oxide layer during high temperature annealing. We will later show that the heat treatment step at a moderate temperature reduces Ge loss. The buried oxide is about 32 nm thick and the original SiGe/Si interface has been substituted by this buried oxide layer. Particularly, the upper interface of the buried oxide (SiGe/SiO_2) is very steep. The Ge signals in the surface oxide and buried oxide layer are negligible because of Ge rejection during surface oxidation and buried oxide formation. Figure 3 shows a scanning electron microscopy (SEM) image of the Auger sputtered crater (about 1 mm wide) on the sample after two-step annealing (800 °C+1350 °C). It is clear from this picture that the interfaces are flat and abrupt, and no apparent defects are visible, confirming the good structure of the obtained SGOI structure.

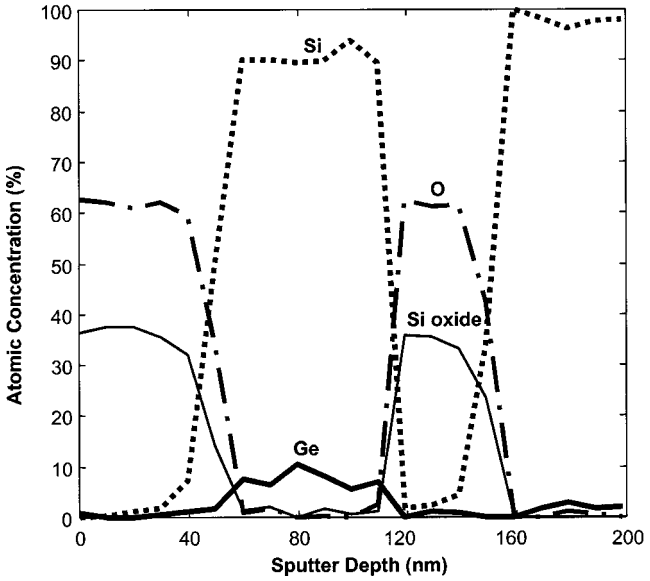

FIG. 2. Elemental depth profiles acquired using sputtering AES from the sample annealed at 800 °C+1350 °C.

Figure 4 shows the Rutherford backscattering spectroscopy (RBS) results acquired from samples after different heat treatment. Figure 4(a) shows the random and aligned spectra for the sample annealed at 800 °C+1350 °C. Signals from channel >550 (mainly between 600 and 800) are Ge signals, among which the peak at 730–770 corresponds to Ge in the SiGe layer and the remnant (left) part is due to diffused Ge into the Si substrate through the implantation-induced-oxygen-rich layer. The valley in the random spectrum at about channel 505 corresponds to the buried oxide layer and the one in the aligned spectrum at about channel 515 originates from SiGe layer. The two peaks at $\sim$300 and $\sim$330 are oxygen signals from the buried oxide and surface oxide layers, respectively. This agrees well with the AES results. The derived channeling yield of the SiGe layer in our SGOI structure is about 30%. Because of the small thickness

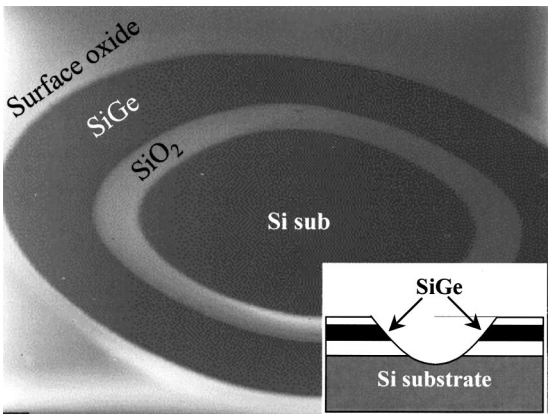

FIG. 3. SEM image of the Auger sputtered crater on the 800 °C+1350 °C sample.

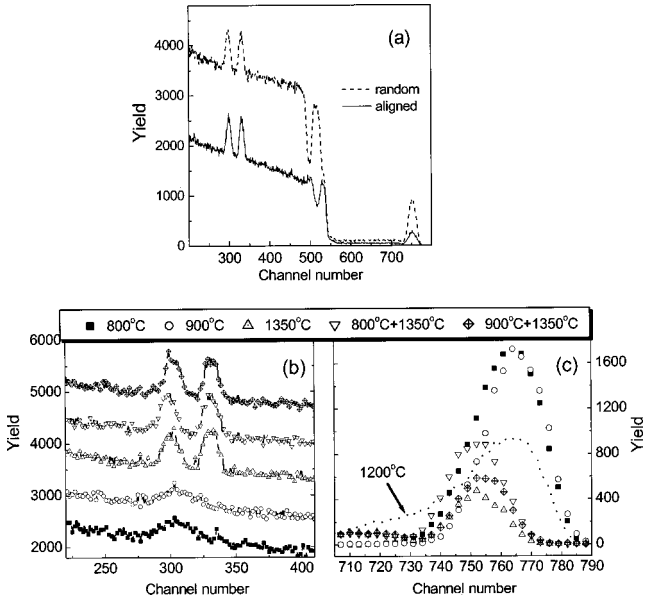

FIG. 4. RBS results acquired from samples after different heat treatment: (a) random and aligned spectra of the sample annealed at 800 °C+1350 °C; (b) and (c) random oxygen signals and germanium signals of different samples (800, 900, 1350, 800 °C+1350 °C and 900 °C+1350 °C). The Ge signals in (b) have been shifted in the vertical direction for clarity. In (c), for comparison, the Ge signal from a sample heated rapidly to 1200 °C and then annealed for 30 min in a furnace.

of the SiGe layer and also its being sandwiched between two amorphous layers (surface oxide and buried oxide), the actual channeling is smaller than 30%. This suggests that the SiGe layer has good crystalline quality. The oxygen signals and Ge signals from samples with different annealing processes are shown in Figs. 4(b) and 4(c). The 800 or 900 °C annealed samples exhibits very little changes compared to the as-implanted sample with a wide oxygen distribution. After annealing at 1350 °C for 5 h, all samples (both single-step annealed and two-step annealed) show narrowed oxygen distribution and also a surface oxide oxygen peak. The Ge band also narrows after 1350 °C annealing resulting from decreased SiGe thickness induced by surface oxidation. This is reasonable since the Ge diffusion coefficient increases by almost ten times for every 100 °C increase in the temperature range of 800–1000 °C and its value at 800 °C is small enough.[12] On the other hand, the intensity of the Ge signals decreases due to Ge penetration through the buried oxide before the establishment of a barrier to Ge diffusion. However, comparing the Ge signals from samples after 1350 °C annealing, the single-step 1350 °C annealed sample shows the weakest Ge peak, and thus the lowest Ge content in the SiGe layer. While the 800 °C+1350 °C annealed sample has the highest remaining Ge content, the 900 °C+1350 °C annealed sample has a lower one, but both are higher than the single-step annealed sample. For comparison, the dotted line in Fig. 4(c) depicts the Ge peak for a furnace-annealed sample with the temperature increased rapidly to 1200 °C and maintained for 30 min. Its peak intensity is already comparable to that of the 800 °C+1350 °C annealed sample. Therefore, the annealing step at a moderate temperature is beneficial to the strengthening of the barrier of the buried oxide against Ge diffusion, and rapid exposure of the as-implanted samples to extremely high temperature should be avoided with regard to Ge diffusion. Our results show that it is possible to depress Ge diffusion into the Si substrate by optimizing the postimplantation heat treatment processing. The decreased Ge content can be retrieved and even further increased by the internal-thermal-oxidation technology[13] or by controlled surface dry oxidation.[14]

Strain relaxation is an important issue for SGOI substrates.[13] The x-ray rocking curve (not shown in this paper) acquired from the sample annealed at 800 °C +1350 °C shows a well-defined diffraction peak from the SiGe layer suggesting that the implantation damage in SiGe layer has been repaired. In accordance with the diffraction peak location and the Ge content determined by AES, the SGOI film is fully relaxed. In comparison, the SiGe diffraction peaks in the rocking curves of samples annealed at 1350 °C and 900 °C+1350 °C are not as well-defined as those of the 800 °C+1350 °C sample. Hence, based on the Ge signals in RBS and rocking curves, the annealing step at a moderate temperature (~800 °C) is important for depressing Ge loss and also the recovery of implantation damage.

In conclusion, we have fabricated relaxed SGOI structures starting from a thin pseudomorphic SiGe material without a buffer layer utilizing a modified SIMOX process. The annealing step at a low temperature (~800 °C) is beneficial for the suppression of Ge penetration, damage recovery in SiGe, and SGOI fabrication.

This work is jointly supported by the special Funds for major state Basic Research Project No. G20000365, National Natural Science Foundation of China under Grant No. 69906005, Shanghai Youth Foundation No. 01QMH1403, as well as Hong Kong RGC CERG CityU 1052/02E or 9040689.

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